WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a memory cell region composed of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said floating gate with the interposition of an interpoly dielectric film, and

a peripheral circuit region having disposed therein a plurality of second MOS field effect transistors, each unitary transistor having a second well region formed in a semiconductor substrate, a second diffusion layer formed in said second well and designed to function as source and drain, and gate electrodes formed on said second well with the interposition of a gate insulating film,

wherein isolation between said plurality of second MOS field effect transistors is effected by shallow groove isolation method, and at least one of said gate insulating films of said plurality of second MOS field effect transistors comprises a first insulating film deposited on the semiconductor

substrate.

2. The memory device according to claim 1 wherein the first insulating film is a silicon oxide film.

3. The memory device according to claim 2 wherein nitrogen is introduced into the silicon oxide film.

4. The memory device according to claim 1 wherein the interpoly dielectric film comprises a second deposited insulating film which is substantially equal to said first insulating film in thickness.

5. The memory device according to claim 4 wherein said first and second insulating films are a silicon oxide film.

6. The memory device according to claim 5 wherein nitrogen is introduced into said silicon oxide film.

7. The memory device according to claim 6 wherein the nitrogen concentration in said second insulating film is higher than that in the first insulating film.

8. A nonvolatile semiconductor memory device comprising:

a memory cell region composed of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor

substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said well with the interposition of an interpoly dielectric film, and

a peripheral circuit region provided with second MOS field effect transistors each having a second well region formed in the semiconductor substrate, a second diffusion layer formed in said second well region and designed to function as source and drain, and first gate electrodes formed on said second well with the interposition of a first gate insulating film, and third MOS field effect transistors each having a third well region formed in the semiconductor substrate, a third diffusion layer formed in said third well region and designed to function as source and drain, and second gate electrodes formed on said third well with the interposition of a second insulating film which is greater than said first gate insulating film in thickness,

wherein isolation in said peripheral circuit region is effected by shallow groove isolation method, and said second gate insulating film comprises a first insulating film deposited on the semiconductor substrate.

9. The memory device according to claim 8 wherein the first insulating film is a silicon oxide

film.

10. The memory device according to claim 9 wherein nitrogen is introduced into the silicon oxide film.

11. The memory device according to claim 8 wherein each of the interpoly dielectric film and the first gate insulating film comprises a second deposited insulating film.

12. The memory device according to claim 11 wherein both of the first and second insulating film are a silicon oxide film.

13. The memory device according to claim 12 wherein nitrogen is introduced into the silicon oxide film.

14. The memory device according to claim 13 wherein the nitrogen concentration in the films is higher in the order of interpoly dielectric film, first gate insulating film and second gate insulating film.

15. A nonvolatile semiconductor memory device comprising:

a memory cell region composed of a memory cell array comprising a plurality of memory cells arranged as a matrix, each memory cell comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a

tunnel dielectric film, and a control gate formed above said floating gate with the interposition of an interpoly dielectric film, and

a peripheral circuit region having disposed therein a plurality of second MOS field effect transistors, each unitary transistor having a second well region formed in the semiconductor substrate, a second diffusion layer formed in said well region and designed to function as source and drain, and gate electrodes formed on said second well with the interposition of a gate insulating film,

wherein isolation between said plurality of second MOS field effect transistors is effected by shallow groove isolation method, and at least one of said gate insulating films of said plurality of second MOS field effect transistors comprises a first insulating film formed by thermally oxidizing the semiconductor substrate and a second insulating film deposited on said first insulating film.

16. The memory device according to claim 15 wherein the first insulating film is smaller than the second insulating film in thickness.

17. The memory device according to claim 15 wherein the second insulating film is a silicon oxide film.

18. The memory device according to claim 17 wherein nitrogen is introduced into the silicon oxide film.

19. The memory device according to claim 15 wherein the interpoly dielectric film comprises a third deposited insulating film which is substantially equal to the second insulating film in thickness.

20. The memory device according to claim 19 wherein the second insulating film and the third insulating film are each a silicon oxide film.

21. The memory device according to claim 20 wherein nitrogen is introduced into the silicon oxide film.

22. The memory device according to claim 21 wherein the nitrogen concentration in the third insulating film is higher than that in the second insulating film.

23. A nonvolatile semiconductor memory device comprising:

a memory cell region composed of a memory cell array comprising a plurality of memory cells arranged as a matrix, each memory cell comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said floating gate with the interposition of an interpoly dielectric film, and

a peripheral circuit region provided with

second MOS field effect transistors each having a second well region formed in the semiconductor substrate, a second diffusion layer formed in said second well region and designed to function as source and drain, and first gate electrodes formed on said second well with the interposition of a first insulating film, and third MOS field effect transistors each having a third well region formed in the semiconductor substrate, a third diffusion layer formed in said third well region and designed to function as source and drain, and second gate electrodes formed on said third well with the interposition of a second insulating film which is greater than said first gate insulating film in thickness,

wherein isolation in said peripheral circuit region is effected by shallow groove isolation method, and the second insulating film comprises a first insulating film formed by thermally oxidizing the semiconductor substrate and a second insulating film deposited on said first insulating film.

24. The memory device according to claim 23 wherein the second insulating film is a silicon oxide film.

25. The memory device according to claim 24 wherein nitrogen is introduced into the silicon oxide film.

26. The memory device according to claim 23 wherein the interpoly dielectric film and the first

gate insulating film comprise a third deposited insulating film which is substantially equal to the second insulating film in thickness.

27. The memory device according to claim 26 wherein the second insulating film and the third insulating film are both a silicon oxide film.

28. The memory device according to claim 27 wherein nitrogen is introduced into the silicon oxide film.

29. The memory device according to claim 28 wherein the nitrogen concentration in the films is higher in the order of interpoly dielectric film, first gate insulating film and second gate insulating film.

30. The memory device according to claim 23 wherein the interpoly dielectric film comprises a third deposited insulating film which is substantially equal to the second insulating film in thickness.

31. The memory device according to claim 30 wherein the second insulating film and the third insulating film are a silicon oxide film.

32. The memory device according to claim 31 wherein nitrogen is introduced into the silicon oxide film.

33. The memory device according to claim 32 wherein the nitrogen concentration in the interpoly dielectric film is higher than that in the second gate insulating film.

34. A process for producing a nonvolatile

semiconductor memory device comprising a plurality of memory cells each having a floating gate formed on a semiconductor substrate with the interposition of a tunnel dielectric film and a control gate formed on said floating gate with the interposition of an interpoly dielectric film, and a plurality of field effect transistors each having gate electrodes formed on the semiconductor substrate with the interposition of a gate insulating film, said process comprising the steps of:

forming a shallow groove isolation region on a semiconductor substrate;

forming a tunnel dielectric film on the semiconductor substrate surface in said memory cell formed region by thermal oxidation method,

depositing a first polycrystalline Si film which becomes said floating gate, and then removing the first polycrystalline Si film in said field effect transistor formed region;

depositing a first silicon oxide film which becomes the first portion of said gate insulating film, and then removing the first silicon oxide film in said memory cell formed region;

depositing a second silicon oxide film which becomes said interpoly dielectric film and a second portion of said gate insulating film; and

depositing a second polycrystalline Si film which becomes said control gate and said gate

electrodes.

35. The process according to claim 34 wherein in the fourth and fifth steps, the first and second silicon oxide films just after deposition are annealed in an NH3 atmosphere and further subjected to wet oxidation.

36. The process according to claim 34 wherein in the third and sixth steps, the first and second polycrystalline Si films are doped with phosphorus.

37. A process for producing a nonvolatile semiconductor memory device comprising a plurality of memory cells each having a floating gate formed on a semiconductor substrate with the interposition of a tunnel dielectric film and a control gate formed on said floating gate with the interposition of an interpoly dielectric film, and a plurality of field effect transistors each having gate electrodes formed on the semiconductor substrate with the interposition of a gate insulating film, said process comprising the steps of:

forming a shallow groove isolation region on the semiconductor substrate;

forming a tunnel dielectric film on the semiconductor substrate surface in the memory cell formed region by thermal oxidation method;

depositing a first polycrystalline Si film which becomes said floating gate, and then removing the first polycrystalline Si film in said field effect

transistor formed region;

forming a first silicon oxide film, which becomes a first portion of said gate insulating film, on the semiconductor substrate surface in the field effect transistor formed region by thermal oxidation method;

depositing a second silicon oxide film which becomes said interpoly dielectric film and a second portion of said gate insulating film; and

depositing a second polycrystalline Si film which becomes said control gate and said gate electrodes.

38. The process according to claim 37 wherein in the fifth step, the second silicon oxide film just after its deposition is annealed in an NH_3 atmosphere and further subjected to wet oxidation.

39. The process according to claim 37 wherein in the third and sixth steps, the first and second polycrystalline Si films are doped with phosphorus.

40. A process for producing a nonvolatile semiconductor memory device comprising a plurality of memory cells each having a floating gate formed on a semiconductor substrate with the interposition of a tunnel dielectric film and a control gate formed on said floating gate with the interposition of an interpoly dielectric film, and a plurality of field effect transistors each having gate electrodes formed on the semiconductor substrate with the interposition

of a gate insulating film, said process comprising the steps of:

forming a shallow groove isolation region on a semiconductor substrate;

depositing a first silicon oxide film which becomes a first portion of said gate insulating film, and then removing said first silicon oxide film in the memory cell formed region;

forming a tunnel dielectric film on the semiconductor substrate surface in the memory cell formed region and forming a second silicon oxide film which becomes a second portion of said gate insulating film between said semiconductor substrate in the transistor formed region and said first silicon oxide film, both by thermal oxidation method;

depositing a first polycrystalline Si film which becomes said floating gate and said gate electrodes;

depositing a third silicon oxide film which becomes said interpoly dielectric film; and

depositing a second polycrystalline Si film which becomes said control gate.

41. The process according to claim 40 wherein in the second and fifth steps, the first and third silicon oxide films immediately after their deposition are annealed in an NH_3 atmosphere and further subjected to wet oxidation.

42. The process according to claim 40 wherein in

the fourth and sixth steps, the first and second polycrystalline Si films are doped with phosphorus.